IN THE CLAIMS:

Please amend claim 1 of pending claims 1-20 as follows:

1 (currently amended): A liquid crystal device (LCD) comprising:

a first substrate;

a second substrate coupled to the first substrate;

a plurality of scan lines and a plurality of data lines arranged over the first substrate, the scan lines intersecting the data lines to define pixel areas;

thin film transistors (TFTs) over the first substrate adjacent intersections of the scan lines and data lines;

~~substantially bilaterally symmetric~~ pixel electrodes respectively arranged in corresponding [~~in the~~] pixel areas such that each pixel electrode is substantially bilaterally symmetric about a vertical reference line crossing the center of the respectively corresponding pixel area in a direction of the data lines; and

a liquid crystal layer interposed between the first and second substrates.

2 (original): The LCD according to claim 1, wherein each of the pixel electrodes has a shape in which a lower right corner and a lower left corner thereof are removed.

3 (original): The LCD according to claim 1, wherein each of the pixel electrodes has a lower center projection extending downwardly.

4 (original): The LCD according to claim 3, wherein each of the pixel electrodes is electrically connected to a TFT at the lower center projection thereof.

5 (original): A liquid crystal display (LCD) including a plurality of scan lines and a plurality of data lines, the scan lines intersecting the data lines to define pixel areas, each of the pixel areas including:

a pixel electrode;

a pair of a first projection and a second projection projecting from an adjacent scan line at one side, the first projection being separated from the second projection;

a thin film transistor (TFT) formed adjacent an intersection of the adjacent scan line and an adjacent data line; and

a storage capacitor connected to the pixel electrode, the storage capacitor including an electrode overlapping with the second projection of the scan line for an adjacent pixel area,

wherein in each of the pixel areas, the pixel electrode has a projection connected to the TFT, the projection of the pixel electrode being disposed between the first projection and the second projection of the adjacent scan line, the pixel electrodes further having a portion overlapping with the scan line for the adjacent pixel area.

6 (original): The LCD according to claim 5, wherein in each of the pixel areas, the first projection is a gate electrode of the TFT.

7 (original): The LCD according to claim 5, wherein in each of the pixel areas, the pixel electrode has a shape avoiding the first projection and the second projection of the adjacent scan line.

8 (original): The LCD according to claim 5, wherein in each of the pixel areas, the electrode for the storage capacitor has a shape projecting towards a lower right part of the pixel electrode in the adjacent pixel area.

9 (original): The LCD according to claim 5, wherein each pixel electrode is substantially bilaterally symmetric.

10 (original): A thin film transistor (TFT) substrate for a liquid crystal display device, the TFT substrate comprising:

a substrate;

a plurality of scan lines over the substrate, extending substantially in a horizontal direction;

a plurality of data lines over the substrate, extending substantially in a vertical direction to intersect the scan lines, the scan lines and the data lines defining an array of pixel areas over the substrate;

a thin film transistor in each pixel area, one terminal of the thin film transistor being connected to one of the adjacent data lines, another terminal of the thin film transistor being connected to one of the adjacent scan lines; and

a pixel electrode in each pixel area, connected to still another terminal of the thin film transistor in the pixel area, the pixel electrode having a pattern configured to yield substantially the same capacitance value for capacitors that are formed between the pixel electrode and the adjacent data line on one side and between the pixel electrode and the adjacent data line on another side.

11 (original): The TFT substrate according to claim 10, wherein the pattern of the pixel electrode is symmetric about a virtual line extending substantially vertically and passing a center of the pixel area.

12 (original): The TFT substrate according to claim 10, wherein the pixel electrode has a substantially rectangular pattern in which a lower right corner and a lower left corner thereof are removed by substantially the same amount.

13 (original): The TFT substrate according to claim 10, wherein each of the pixel areas includes a storage capacitor connected to the pixel electrode for the pixel area.

14 (original): The TFT substrate according to claim 13, wherein an area occupied by the storage capacitor for a pixel area extends into an adjacent pixel area.

15 (original): The TFT substrate according to claim 14, wherein each pixel area has a space between the pixel electrode and one of the adjacent data lines, and

wherein the area occupied by the storage capacitor for a pixel area extends into such a space in an adjacent pixel area.

16 (original): The TFT substrate according to claim 15, wherein each pixel area includes a projection projecting from the adjacent scan line that is connected to the TFT in the pixel area, and

wherein the storage capacitor for a pixel area is constructed at least in part by the projection of the scan line for an adjacent pixel area.

17 (original): The TFT substrate according to claim 16, wherein each pixel area has an electrode for the storage capacitor, the electrode for the storage capacitor for a pixel area overlapping with the scan line for an adjacent pixel area and the projection thereof.

18 (original): The TFT substrate according to claim 17, wherein the pixel electrode in each of the pixel areas has a portion overlapping with the scan line for an adjacent pixel area, and

wherein the storage capacitor for the pixel area is constructed at least in part by the portion of the pixel electrode that overlaps with the scan line for the adjacent pixel area.

19 (previously presented): The TFT substrate according to claim 10, wherein each pixel area has spaces between the pixel electrode and adjacent data lines, and the area of the space between the pixel electrode and one of the adjacent data lines is substantially the same as the area of the space between the pixel electrode and another one of the adjacent data lines.

20 (original): The TFT substrate according to claim 19, wherein each pixel area includes a storage capacitor connected to the pixel electrode for the pixel area, and

wherein an area occupied by the storage capacitor for a pixel area extends into an adjacent pixel area.